In re Patent Application of:
WALTERS ET AL
Serial No. **10/696,138**
Filed: **10/29/2003**

REMARKS

Original Claims 1-13 have been replaced by new Claims 14-17 in an effort to more concisely defined applicants' invention, in a manner that is believed to patentably distinguish over the patent to Kates, 6,577,515, cited in support in the rejections under 35 U.S.C. 102 and 35 U.S.C. 103, in the outstanding office action. Reconsideration of this application in light of the foregoing amendments and following remarks is respectfully requested.

Before discussing the differences between applicants' claimed invention and the prior art relied upon in the outstanding office action, the invention will be briefly reviewed, in order that differences between the patent to Kates and the invention claimed in replacement Claims 14-17 may be more readily appreciated.

As is described briefly beneath the header "Summary of the Invention", the subject matter of the present invention involves a combination of one or more fast response time-base converter channels and one or more highly efficient converter channels, the outputs of which are combined to result in a composite output current.

As is shown in Figure 1 of the drawings of the present application and as is described in paragraph [011] on page 5 of the present specification, for each of the respective channels, including both the high efficiency channel and the fast response time channel, the output of an integrating error amplifier 20 is monitored by respective drive and control circuits that controllably supply drive signals to associated MOSFET switching pairs. A common clock is used to drive the pair of fast channels

30-2 and 30-3, while a divided clock through divider 55 is used to drive the high efficiency 30-1.

A key feature of the present invention, which is now believed to be more concisely defined in the replacement claims, is a fact that the invention employs a single control loop for controlling the operation of both the high efficiency channel and the fast response time channel.

As is described in paragraph [014], with the high efficiency channel being used to supply 100% of the leakage current, each of the two fast response channels is controlled so as to handle one-half of the high load current demand. In other words, both the high efficiency channel and the fast response time channel are simultaneously and continuously enabled by the single control loop, so as to appropriately drive the respective channels to handle the current demand at the output node. What is produced is a low current composite produced by a combination of the outputs of the high efficiency channel and the fast response time channel.

In replacement Claims 14-17 these features of the present invention are believed to be concisely defined by specifying that the high efficiency channel and the one or more fast response time channel are controlled by way of a single control loop, which monitors the output node and simultaneously and continuously enables each of the high efficiency channels and then one or more fast response time channels, so as to cause the high efficiency channels to supply 100% of leakage current for a light load condition, and, in response to a dynamic increase in current demand from the leakage value to a full load current value, the one or more fast response time channels responds by handling the full load current so as to realize a composite load

current at the output node comprised of the leakage current and the full load current.

Looking now at the prior art cited in the outstanding office action, the power supply described in the patent to Kates, 6,577,515, employs a standard converter 125 and a fast response converter 150, the latter being controlled by a dedicated control circuit 175.

As described in column 2, lines 48-54, the fast response time converter 150 is disabled during normal operation of the power supply. However, when a transient voltage event occurs, the fast response converter 150 may be enabled by its associated control circuit 175 depending upon the voltage at the output node. Once the output voltage returns to a specified value, the fast response time converter is disabled.

In effect, Kates employs two separate control loops, one for the normal converter, and a second for the fast response time converter. The control loop for the fast response time converter selectively turns that converter on and off.

In contrast therewith, the present invention employs only a single control loop, which monitors the output node and provides control signals to each of the drive and control circuits for the fast channels and the efficient channel. Because they are enabled, the fast channels will respond rapidly to a substantial increase in output load current by rapidly meeting the demand for increased load current.

Moreover, the use of a single control loop in accordance with the present invention avoids the problem of having two control loops as in Kates which may tend to fight one another depending upon load current.

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In the absence of a citation of prior art which teaches or suggests controlling both a high efficiency channel and one or more fast response channels by means of a single control loop to produce a single composite output signal combined from the two, as defined in replacement Claims 14-17, it is respectfully submitted that the present application in condition for allowance.

Favorable reconsideration of this application and a notice of allowablity of Claims 14-17 are, accordingly, earnestly solicited.

Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to Deposit Account No. 01-0484 and please credit any excess fees to such deposit account.

Respectfully submitted,

CHARLES E. WANDS
Reg. No. 25,649

Customer No.: 27975

Telephone: (321) 725-4760

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number **571-273-8300** to MAIL STOP AMENDMENT, COMMISSIONER FOR PATENTS, this 31st day of August 2005.

J. Kallemeyn